Digital alternative posed to conventional RF

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Designers of radio circuits on advanced CMOS processes at Texas Instruments Inc. have recognized a new paradigm: In a deep-submicron CMOS process, the time-domain resolution of a digital signal edge transition is superior to the voltage resolution of analog signals. That calls for an architecture in which an all-digital frequency synthesizer and transmitter, as well as a digitally intensive discrete-time receiver, are the foundation for a digital RF processor that exploits fast switching times and fine capacitor ratios, while avoiding problems related to voltage headroom.

A transceiver that is readily integrated with a digital baseband and application processor is described here. It replaces the conventional RF synthesizer architecture, based on a voltage-controlled oscillator and a phase/frequency detector and charge-pump combination, with a digitally controlled oscillator (DCO) and a time-to-digital converter (TDC). The DCO avoids all analog tuning controls. All inputs and outputs are digital at 2.4 GHz; the 40-ps rise time makes almost a perfect square wave. The advanced lithography allows creation of extremely fine variable capacitors (varactors)-about 40 attofarads of capacitance per step, which equates to the control of only 250 electrons entering or leaving the resonating inductor-capacitor tank.

Fast switching

Despite the small capacitance step, the resulting frequency step at the 2.4-GHz RF output is 23 kHz-too coarse for wireless applications. We thus resorted to the fast switching capability of the transistors by performing high-speed 600-MHz sigma-delta dithering of the 250 electrons in the finest varactors. The duty cycle of the high/low capacitive states establishes the time-averaged resonating frequency resolution, now less than 1 kHz.

The TDC has a fine time resolution of one inverter delay, which could be in the low tens of picoseconds. It is realized by passing the DCO digital output through the 32-inverter chain and sampling the inverter outputs. The digital logic circuitry directly performs phase-locked loop (PLL) operation on the 2.4-GHz local oscillator output clock.

The transmitter architecture is fully digital and takes advantage of the wideband frequency modulation capability of the all-digital PLL by adjusting its digital frequency command word. The modulation method is an exact digital two-point scheme, with one feed directly modulating the DCO frequency deviation while the other is compensating for the developed excess phase error. The DCO gain characteristics are constantly calibrated through digital logic to provide the lowest possible distortion of the transmitted waveform.

The power amplifier comprises a multitude of digital NMOS switches followed by a matching network. The RF amplitude is regulated by controlling the number of active switches. Despite the high speed of digital logic operation, the overall power consumption of the transmitter architecture measured in a Bluetooth radio is about half that of architectures to date.

The receiver uses direct RF sampling with discrete-time signal processing. The incoming RF signal is strengthened and converted into current by a low-noise amplifier, which is the only analog continuous-time circuit in the entire RX chain. The RF current is then sampled at the Nyquist rate, thus creating 2.4-GHz charge packets. The RF charge packets undergo several cycles of filtering and downconversion. During charge accumulation, splitting and combining, the discrete-time signal processing of temporal FIR filtering, IIR filtering and spatial FIR filtering is brought forth.

The precise capacitor ratio property of the deep-submicron CMOS is used. After significant removal of interferers, the charge packets are converted to digital format by the sigma-delta A/D converter, followed by the digital decimating filters.

Application of the presented ideas has resulted in drastic cost, area and power savings for Bluetooth radios, and the digital RF processor design is further being used in demonstrations of a GSM/GPRS cellular application. It also serves as a foundation for a software-defined radio.

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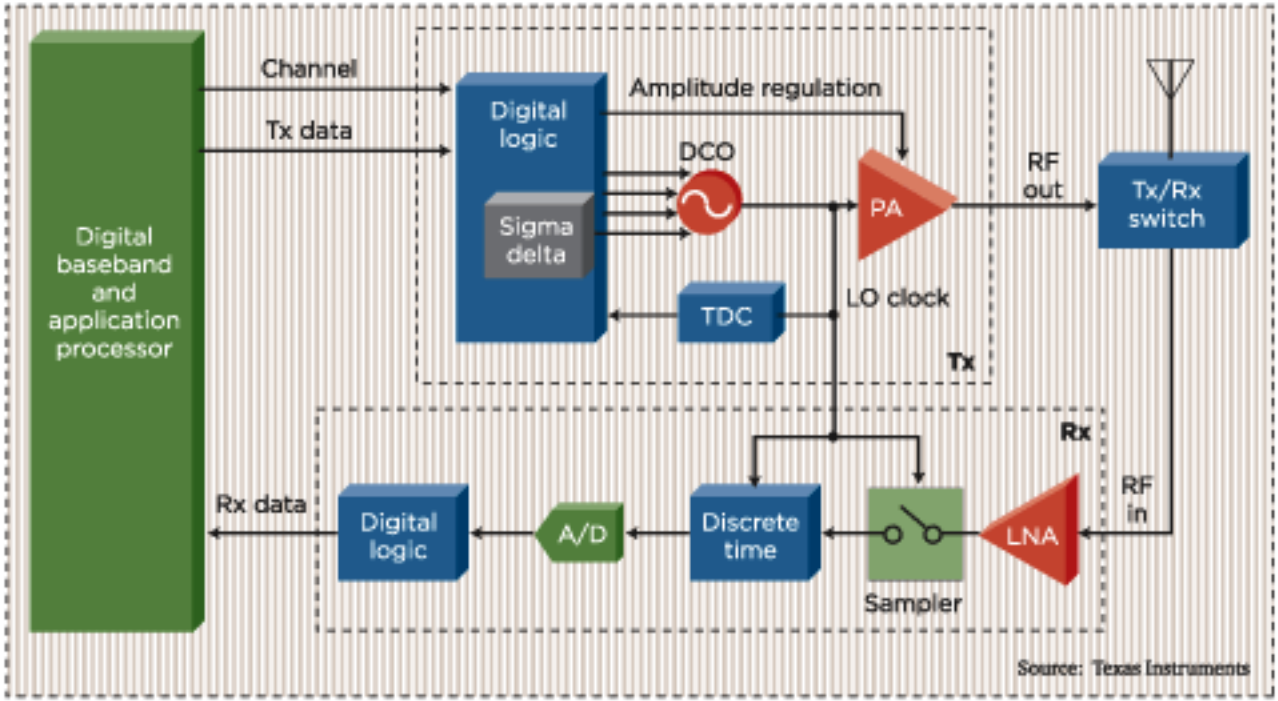
See related chart



To leverage fully the attributes of a deep-submicron CMOS process, a novel transceiver architecture has been demonstrated that comprises an all-digital frequency synthesizer and transmitter as well as a digitally intensive discrete-time receiver.